OIPE
FEB 26 2002
PATENT & TRADEMARK OFFICE
JC98

2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Nobutoshi AOKI Attorney Docket 40301/0578

Title: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING INSULATED GATE FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING THE SAME

Appl. No.: 09/440,928

Filing Date: November 16, 1999

Examiner: S. Rao

Art Unit: 2814

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TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is a Preliminary Amendment in the above-captioned application. The fee has been calculated as shown below. *(Small entity fees indicated in parentheses.)*

CLAIMS AS AMENDED						
(1)	(2)	(3)	(4)	(5)	(6)	(7)
	Claims Remaining After Amendment		**Highest Number Previously Paid For**	**Extra Claims**	**Rate**	**Fee**
Total Claims	31	-	27	4	18.00	**$72.00**
(Small Entity)					*(9.00)*	
Independent claims	10	-	9	1	84.00	**$84.00**
(Small Entity)					*(42.00)*	
Multiple Dependent		-			280.00	
(Small Entity)					*(140.00)*	
Extension of Time	**One Month**		**Two Months**	**Three Months**	**Four Months**	
Fee	$110		$400	$920	$1,440	
(Small Entity)	*($55)*		*($200)*	*($460)*	($720)	
Total Fees						**$156.00**

A check in the amount of the above Total Fees is attached. This amount is believed to be correct; however, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 19-0741.

Respectfully submitted,

Aaron C. Chatterjee

Aaron C. Chatterjee
Reg. No. 41,398

Date: February 26, 2002

FOLEY & LARDNER
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Attorney Docket 040301-0578

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Applicant: Nobutoshi AOKI et al.

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AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In reply to the Office Action mailed November 26, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims by replacing the indicated claims with the following clean versions. (See **Attachment A** for the marked up version of the amended claims.)

Sub B1
A1 Cont.

1. (Amended) A semiconductor device comprising:

a pair of main electrodes used as source and drain electrodes;

an insulating gate film adjacent to the pair of main electrodes; and

a gate electrode comprising of a first region composed at least a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region composed of the first group IV element and formed on the first region.

03/04/2002 SSITHIB1 00000033 09440928
01 FC:102 84.00 OP
02 FC:103 72.00 OP